REMARKS

Claims 1-13 are presently pending in the application.

The Office Action rejected claims 1 and 5-12 under 35 U.S.C. 102(e) as being anticipated by Kobayashi et al. (U.S. Patent No. 6,797,566), and rejected claims 2-4 under 35 U.S.C. 103(a) as being unpatentable over Kobayashi et al. as applied to claim 1 and further in view of Tsui et al. (U.S. Patent No. 6,208,030). Applicants respectfully traverse these rejections.

Regarding the rejection of independent claim 1 as being anticipated by Kobayashi et al. it is well established that "[a] claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." (Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987)). Thus, for a rejection under 35 U.S.C. 102(e) to be proper, every limitation recited in a claim, which is rejected as being anticipated by a prior-art reference, must be clearly disclosed in that single prior-art reference. In the instant case, Applicants respectfully submit that the cited Kobayashi et al. reference does not disclose each and every element of rejected claim 1, and, therefore, the cited Kobayashi et al. reference does not anticipate the presently pending claims under 35 U.S.C. § 102(e).

More particularly, applying the above standard to claim 1, Kobayashi et al. does not disclose a method for forming at least one non-volatile memory cell including, among other things, "forming a first oxide layer, an electron trapping layer, a second oxide layer, a first electrically conductive layer, and a dielectric layer on a surface of a substrate in that order; patterning ... thereby forming at least one component stack; depositing a third oxide layer ... ; removing a portion of an upper section ... such that an upper portion of the dielectric layer is exposed through the third oxide layer; removing ... such that an elevation of an upper surface of the third oxide layer above the surface of the substrate is substantially equal to an elevation of an upper surface of the patterned first electrically conductive layer; and forming a second electrically conductive layer over upper surfaces of the patterned first electrically conductive layer and the third oxide layer," as recited in independent claim 1.

According to the Office Action, Kobayashi et al. anticipates the language of claim 1 as follows:

> A method for forming at least one non-volatile memory cell, comprising:
>
> forming a first oxide layer (202), an electron trapping layer (206; col. 8, lines 45-60), a second oxide layer (208), a first electrically conductive layer (209), and a dielectric layer on a surface of a substrate (210) in that order (Fig. 5(a-e);
>
> patterning the dielectric layer and the first electrically conductive layer, thereby forming at least one component stack (col. 9, lines 40-55);
>
> depositing a third oxide layer over and beside the at least one component stack (Fig. 11 (214') and col. 13, lines 33-40);
>
> removing a portion of an upper section of the third oxide layer opposite the second oxide layer such that an upper portion of the dielectric layer is exposed through the third oxide layer (col. 13, lines 33-40); ....

Regarding the Kobayashi et al. patent, Fig. 3(a) to Fig. 5(e) depict a sequence of successive processing steps with Fig. 3(a) being the first step of the sequence and Fig. 5(e) being the last step of that sequence. Now, looking at the Office Action's application of Kobayashi et al. to the reproduced language of claim 1, the above-asserted "forming" step would apparently need to occur by way of a series of steps spanning Fig. 3(a) to Fig. 5(d). Next, the above-alleged "patterning" step would apparently need to be interpreted as occurring at Fig. 5(e).

Next, the Office Action interprets the following "depositing" step as occurring at Fig. 11. The problem with this interpretation would appear to be that the steps of Fig. 11 occur before the step of Fig. 4(c). Col. 13, lines 41 and 42 state that the steps of Fig. 11 occur before the steps of Fig. 10(b) et seq., and as described in col. 13, lines 9-15 the steps of Fig. 10(b) et seq. occur before the steps of Fig. 4(c). Consequently, since the component stack is allegedly formed at Fig. 5(e), the steps of Fig. 11 (which occur before Fig. 4(c)) would appear to be interpreted by the Office Action as occurring before the component stack even exists. It would thus appear to

be nonsensical for a "third oxide layer" to be deposited "over and beside the at least one component stack" when the component stack has not yet even been formed.

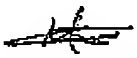
Furthermore, regarding the above "removing" step, the Office Action's interpretation of the "third oxide layer" (214') being disposed "opposite the second oxide layer" (208) would appear to be without merit, since Kobayashi et al. discloses the layer 214' being formed before layer 208. In particular, layer 208 would allegedly be formed at step 4(c) but the formation of layer 214' in Figs. 11(a-b) would allegedly occur before Fig. 4(c). Col. 13, lines 41 and 42 state that Figs. 11(a-b) occur before Fig. 10(b) et seq., and as described in col. 13, lines 9-15 the steps of Fig. 10(b) et seq. occur before the steps of Fig. 4(c). Accordingly, it would thus not appear to be possible for the process of Kobayashi et al. to perform a step of "removing a portion ... of the third oxide layer [214'] opposite the second oxide layer [208]" since layer 208 would apparently not even exist until well after layer 214' had already been formed. Additionally, for similar reasons, it would not appear to be possible for the process of Kobayashi et al. to perform a step of "removing a portion ... of the third oxide layer [214'] ... such that ... the dielectric layer [210] is exposed through the third oxide layer" since the dielectric layer 210 also would not yet exist (furthermore, as discussed above, the third oxide layer would not exist at this time either). Moreover, the two layers 208 and 214a' would appear not to be operable together (i.e., would appear to be mutually exclusive) after step 4c has occurred. In other words, the First Embodiment of Kobayashi et al. uses silicon oxide film 208 in steps 4(c-d) and the Third Embodiment of Kobayashi et al. appears to use silicon oxide film 214a' instead of silicon oxide film 208, so that the two films would not appear to exist together in a single embodiment of the allegedly claimed "removing" step.

Additional inconsistencies of an interpretation of Kobayashi et al as applied to the remaining steps of claim 1 would appear to exist; Applicants invite the Examiner to contact Applicants' representative, listed below, by phone to discuss these further issues should the above examples not be sufficient. In view of the above, Applicants submit that the Office Action's reading of Kobayashi et al. would appear to be flawed so that the rejection of claim 1 under 35 U.S.C. 102(e) would appear to be without merit. The presently pending dependent claims would thus appear to be allowable, as well, at least because of their dependencies on

claim 1. It is respectfully requested that the rejections of all of the claims under 35 U.S.C. 102(e) and 103(a) be reconsidered and withdrawn.

In view of the above, Applicants submit that the application is now in condition for allowance, and an early indication of the same is requested. The Examiner is invited to contact the undersigned with any questions.

Respectfully submitted,



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September 20, 2005
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